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Analysis of Mueller–Muller Clock and Data Recovery Circuits with a Linearized Model

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Abstract: With the development of high-speed analog-to-digital converter (ADC)-based wireline receivers, the Mueller–Muller clock and data recovery (MM-CDR) circuit has garnered increasing attention. But in the design stage, evaluating the loop performance of MM-CDR circuits in ADC-based wireline receivers is challenging due to the absence of a linearized model for a Mueller–Muller phase detector (MMPD). In this paper, a linearized model of the MMPD is proposed by analyzing the output probability of the MMPD in different transition patterns with random jitter injection, and the model is combined with an entire MM-CDR system to analyze the performance of the MM-CDR loop. Analysis of the linearized model and corresponding simulations indicate that when the reference voltage level in the MMPD is set equal to the amplitude of the average crossing voltage at the intersection of 011 and 110 patterns, the MMPD can obtain the maximum gain, which is determined by jitter, and the jitter transfer function and jitter tolerance can achieve optimum performance.

Keywords: clock and data recovery; Mueller–Muller phase detector; linearized model; jitter tolerance

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1. Introduction

With the great improvement of data transmission rate requirements under severe channel impairments, the analog-to-digital converter (ADC)-based wireline receiver (RX) receives more and more attention because of its flexible and powerful equalization capability. The sampling clock of the ADC is adjusted by the clock and data recovery (CDR) circuit. The classical Bang-Bang phase detector (PD) is no longer the best choice for the high-speed CDR circuit because of its requirement for double oversampling information, which consumes excessive power in ADC-based architecture. Therefore, the baud-rate CDR has been used increasingly in ADC-based high-speed wireline receivers. The baud-rate CDR only collects one sample per unit interval (UI), so the rate requirement of the sampling clock is halved compared with the Bang-Bang PD (BBPD). Baud-rate CDR usually adopts a Mueller–Muller phase detector (MMPD) to determine the optimal sampling phase of the ADC clock [1–3].

The intuitive understanding of the performance of the CDR loop is whether it can provide an optimal sampling phase for the ADC to make the wireline transceiver system achieve the lowest bit error rate (BER). During testing, CDR performance can be assessed through BER results. However, in simulation, it is difficult to verify the BER requirements of 1×10^{-12} or even 1×10^{-15} for communication protocols. Thus, we cannot obtain the performance of the CDR through time-domain simulation during the design stage. Consequently, during the design stage, CDR performance can only be analyzed by linearizing the CDR loop. Such an analysis method has been widely used in Bang-Bang CDR (BB-CDR) [4–8], In [4], Sonntag et al. presented a general architecture for digital clock and data recovery for high-speed binary links and provided a linearized analysis of the BBPD and CDR loop. For the baud-rate CDR architecture, a lot of work has analyzed its performance [9–12]. In [10], Han et al. combined current integration in the front end for energy-efficient equalization with integration phase dithering to realize a robust baud-rate

CDR and analyzed the performance of the CDR loop by adding dither information. In [11], Lee et al. generated the reference level for phase error detection from the consecutive identical bits (such as 011 or 110 pattern) in its proposed PD architecture and completed the analysis of the CDR loop performance through the probability density function (PDF) of the three-bit pattern. In [12], Park et al. proposed pattern-based PD considering three consecutive data and one error, which increases the density of transition to be detected to twice that of a conventional MMPD.

However, the performance of baud-rate Mueller–Muller CDR (MM-CDR) cannot be analyzed because of the lack of a linearized model of an MMPD in previous works; these studies only focused on the application of MM-CDR without a systematic analysis [13–17]. For example, in [13], Francese et al. modified the lock point of MM-CDR to the unequalized pulse response. In [16], Choi et al. adopted a weight-adjusting sign–sign MM-CDR with the maximum-eye tracking algorithm to make the CDR lock at the optimal phase that maximizes the eye height. To solve this problem, Liu et al. proposed a linearized model for a MM-CDR for the first time [18]. They introduced drift bit width to characterize an MMPD. However, this study lacked analysis of the relationship between reference voltage and drift bit width and the impact of different reference voltages on the performance of the CDR loop.

In this work, we investigate the influence of the reference voltage on the MMPD by proposing a segmented linear function to model the relationship between voltage and phase and finally propose a linearized model for MM-CDR. This article has the following organization. Section 2 delineates the working principle of the MMPD and the linearization of the MMPD. Section 3 details the small signal model of MM-CDR followed by Section 4, which exhibits the simulation results of the MM-CDR. Finally, Section 5 summarizes the conclusions.

2. Mueller–Muller Phase Detector

2.1. The Principle of MMPD

The MMPD infers the channel response from baud-rate samples of the received data, and the adaptation aligns the sampling clock such that the pre-cursor is equal to the post-cursor in the pulse response defined in [1]. The timing function $f(\tau)$ is expressed as

$$f(\tau) = \frac{1}{2}(h_1 - h_{-1}) = \frac{1}{2}[h(\tau + T) - h(\tau - T)] \quad (1)$$

where $h(\tau)$ is the pulse response of the system, and h_0, h_1 and h_{-1} represent the amplitude of the current-cursor, post-cursor and pre-cursor, respectively. The result of the sampling instant for a pulse is shown in Figure 1. Algorithms will choose their steady-state timing in such a way as to yield equal echoes h_1 and h_{-1}. If h_1 is greater than h_{-1}, the sampling time of CDR is early. Similarly, if h_1 is smaller than h_{-1}, the sampling time of CDR is late.

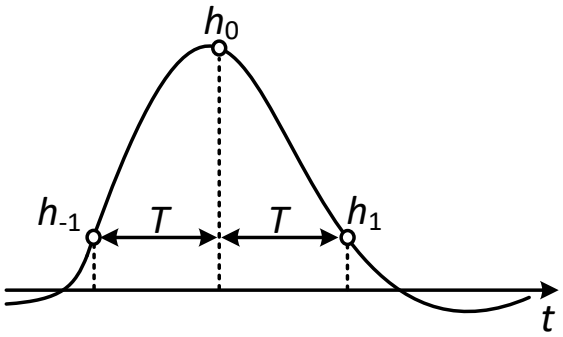


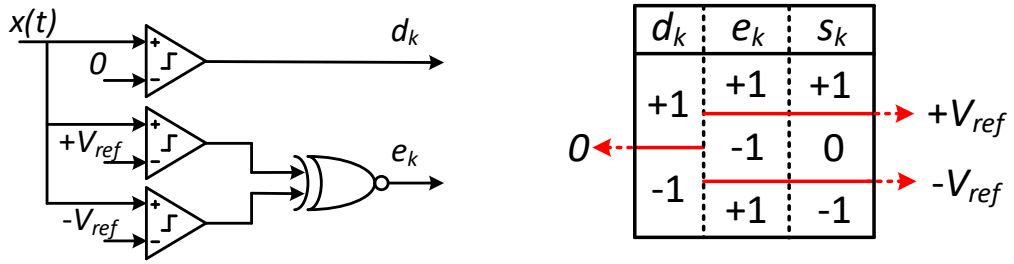
Figure 1. The sampling instant with $2f(\tau) = (h_1 - h_{-1})$ timing function.

The generation of the MMPD timing estimator z_k for the binary signaling format defined in [1] is shown in Figure 2a, and its expression is

$$z_k = \frac{1}{2}(x_k d_{k-1} - x_{k-1} d_k) \tag{2}$$

where x_k is the input analog samples and d_k is the signal decision value which can only be values of ± 1. And the expectation is

$$E\{z_k\} = \frac{1}{2}(h_1 - h_{-1}). \tag{3}$$



(**a**) (**b**)

Figure 2. (**a**) The generation diagram of the MMPD timing estimator z_k. (**b**) The value of d_k, e_k and s_k.

Thus, the timing function $f(\tau)$ is transformed into the expectation of timing estimator z_k. The analog samples x_k are converted to digital signals s_k after ADC. For simplicity, at least we can use two-bit s_k to express the input signal, as shown in Figure 2b. Thus, s_k can be expressed with d_k and e_k as

$$s_k = \frac{d_k(e_k + 1)}{2} \tag{4}$$

where e_k is the error signal generated by the comparison between x_k and $\pm V_{ref}$. Then, the MMPD timing estimator z_k can be converted to

$$z_k = \frac{x_k d_{k-1} - x_{k-1} d_k}{2} \sim \frac{s_k d_{k-1} - s_{k-1} d_k}{2} = \frac{d_k d_{k-1}(e_k - e_{k-1})}{4}. \tag{5}$$

Equation (5) illustrates how the phase error is detected based on the sign of two consecutive samples and the sign of two consecutive errors. The waveform diagram of phase error detection is shown in Figure 3, and the phase error values are listed in Table 1.

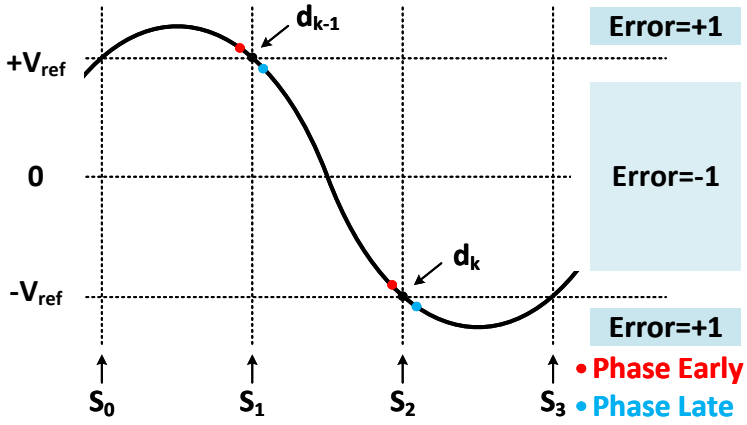


Figure 3. The phase error generation of the MMPD.

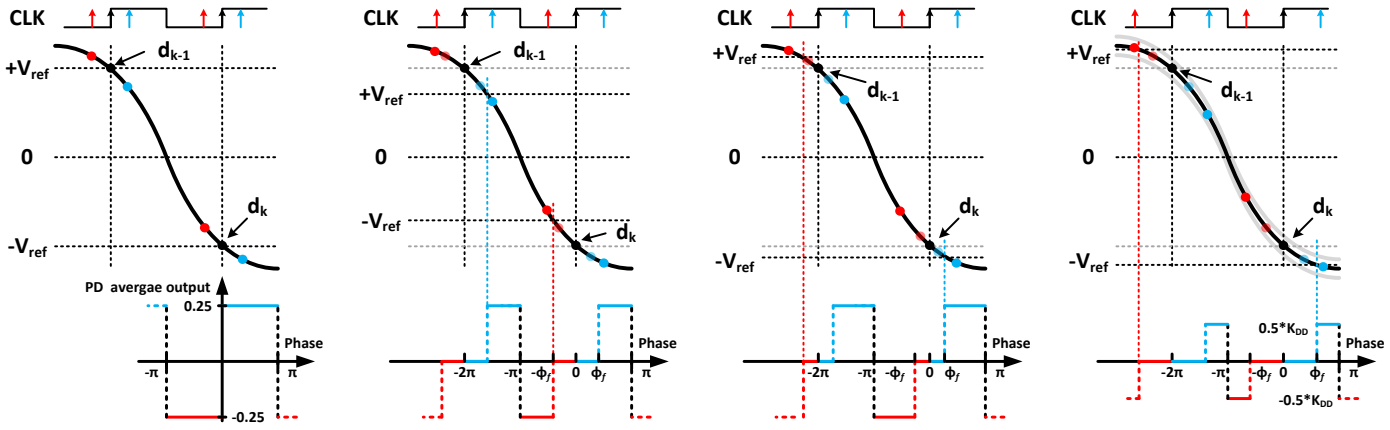
Table 1. Truth table of the MMPD.

d_k	d_{k-1}	e_k	e_{k-1}	Phase Error
1	−1	1	−1	Late
−1	1	1	−1	Late
1	−1	−1	1	Early
−1	1	−1	1	Early
All other cases				Hold

2.2. The Influence of the Reference Voltage

Compared to BBPD, the MMPD needs two more comparisons between the input and reference voltage $\pm Vref$, respectively, which influences the MMPD output directly. Considering that the output of the MMPD has judgments of late and early, we assign "1" to late and "−1" to early.

Figure 4 illustrates the MMPD output characteristic at different reference voltage values. When the value is appropriate, all phase error information can be output correctly, as shown in Figure 4a. The MMPD average output value is equal to the product of data transition density (K_{TD}) and average detection density (K_{DD}), where K_{TD} can be assumed to 0.5 for random data and the K_{DD} is 0.5 in a conventional MMPD, because only half of the transitions can be detected [12].



(**a**) (**b**) (**c**) (**d**)

Figure 4. MMPD output characteristic (red: phase early, blue: phase late) (**a**) reference voltage is appropriate, (**b**) reference voltage is lower than appropriate value, (**c**) reference voltage is higher than appropriate value, (**d**) reference voltage is too higher to detect all transition.

However, if the reference voltage is lower than the appropriate value, there is a fuzzy phase region where the phase error information cannot be captured correctly, as shown in Figure 4b. This occurs because in the generated error signal, both e_k and e_{k-1} are +1 in this region, which gives "hold" information as defined in Table 1. Only when the sample phase offset is larger than the fuzzy phase ϕ_f, PD captures the phase error information. On the other hand, when the reference voltage is higher than the appropriate value, there is also a fuzzy phase region, because both e_k and e_{k-1} are -1 in this region, as shown in Figure 4c. If the reference voltage is even higher, as shown in Figure 4d, some transition will be lost because of the previous bits residual state, which lowers the detection density.

2.3. Linearization of MMPD

To facilitate the analysis of the MM-CDR loop performance during the design stage, it is essential to linearize the MMPD. Previous works have developed linearized models for BBPD by incorporating jitter sources such as random jitter (RJ) and deterministic jitter (DJ) [4–7]. Similarly, these jitter sources smooth the ideal non-linear output of the MMPD

and enable the gain of the MMPD to be linearized. Since RJ originates from device noise such as thermal noise, flicker noise and shot noise, it is usually modeled as a Gaussian distribution with zero-mean. In communication protocols, its standard deviation (STD) is typically required to be less than 0.02 UI or even 0.01 UI. DJ is mainly composed of a previous bits residual state, duty cycle distortion and sinusoidal jitter, which originate from the lossy channel, mismatched rise and fall time, and spread spectrum clocking, respectively.

Considering the entire data transmission process of n bits, the average output μ of the MMPD represents the mean probability of detecting "late" or "early" for each bit:

$$\mu = \frac{\sum_{k=1}^{n} \Big((1)Pr(late|d_k|\phi) + (-1)Pr(early|d_k|\phi) \Big)}{n} \tag{6}$$

where d_k represents the k-th bit data, and ϕ represents the phase offset between the ideal sampling phase and actual sampling phase.

For a 0-1 transition pattern, there are four cases if considering an additional 2 bits before and after it, which include the "0011", "1011", "0010" and "1010" transition pattern. So, Equation (6) can be written as:

$$\mu = Pr(C_k) \cdot (Pr(late|C_k|\phi) - Pr(early|C_k|\phi)) \tag{7}$$

where $Pr(C_k)$ is the probability of case k (k = 1, 2, 3, 4).

Assuming Gaussian jitter with zero-mean and standard deviation σ is added to the phase error, as shown in Figure 5, we define ϕ_{f1} as the fuzzy phase region for consecutive transition patterns like the 0101 pattern or the third bit "1" in the 0010 pattern, and we define ϕ_{f2} as the fuzzy phase region for consecutive same data like the 0011 pattern or the second bit "0" in the 0010 pattern. The fuzzy phase region is the phase offset between the ideal sampling phase and the cross-point of the reference voltage and the transition edge.

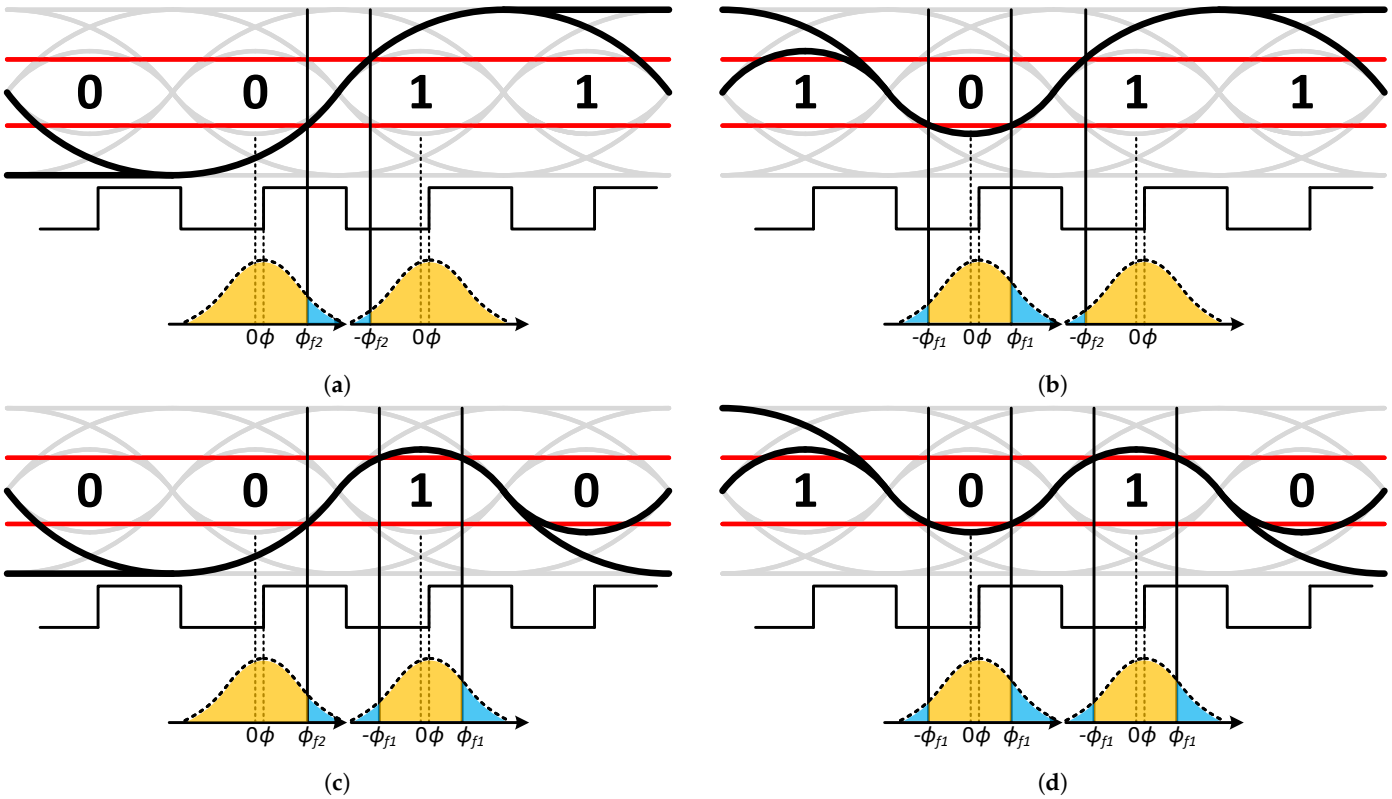


Figure 5. Transition pattern with jitter injection (orange region: error signal is +1, blue region: error signal is −1) (**a**) case 1: 0011 , (**b**) case 2: 1011, (**c**) case 3: 0010, (**d**) case 4: 1010.

The probability of late $Pr(late|\phi)$ is equal to the product of the probability of $e_k = +1$ multiplied by the probability of $e_{k-1} = -1$. For case 1, it is

$$Pr(late|\phi|C_1) = \int_{-\phi_{f2}}^{\infty} \frac{1}{\sigma\sqrt{2\pi}} e^{\frac{-(x-\phi)^2}{2\sigma^2}} dx \cdot \int_{\phi_{f2}}^{\infty} \frac{1}{\sigma\sqrt{2\pi}} e^{\frac{-(x-\phi)^2}{2\sigma^2}} dx. \tag{8}$$

Let $y = \frac{x-\phi}{\sigma}$; then, we have

$$\begin{aligned} Pr(late|\phi|C_1) =& \frac{1}{\sqrt{2\pi}} \int_{\frac{-\phi_{f2}-\phi}{\sigma}}^{\infty} e^{-\frac{y^2}{2}} dy \cdot \frac{1}{\sqrt{2\pi}} \int_{\frac{\phi_{f2}-\phi}{\sigma}}^{\infty} e^{-\frac{y^2}{2}} dy \\ =& \Phi\left(\frac{\phi_{f2}+\phi}{\sigma}\right) \cdot \Phi\left(\frac{-\phi_{f2}+\phi}{\sigma}\right) \end{aligned} \tag{9}$$

where $\Phi(x)$ is the cumulative distribution function of the standard normal distribution. The probability of early and probability of late in other cases can be calculated in a similar way. For random data, the probability of the four cases mentioned is 1/16. In addition, the analysis will be no different for an inverted data pattern. Substituting these four cases' calculation results into Equation (7), we have

$$\mu = \frac{\Phi\left(\frac{\phi_{f2}+\phi}{\sigma}\right) - \Phi\left(\frac{\phi_{f2}-\phi}{\sigma}\right)}{4}, \tag{10}$$

which is 0.25 if there is no jitter, being the same as we mentioned in Section 2.2.

There is no ϕ_{f1} in Equation (10), which indicates that the transition before or after the consecutive same data (00 or 11) actually plays a role in the MMPD. We give a qualitative explanation here: when data continuously transition, e_k and e_{k-1} will always be the same (both are +1 or -1). Therefore, in case 1, there is one judgment for a phase late or early in the transition and K_{DD} is 1. In case 2, only an early phase can be judged, because e_k and e_{k-1} are -1 when the phase is late, which cannot be judged in a conventional MMPD. Similarly, in case 3, only a late phase can be judged. So, K_{DD} in case 2 and case 3 is 0.5. The MMPD output is 0 in case 4, and its K_{DD} is 0. Therefore, the average K_{DD} is 0.5 for a conventional MMPD. Without loss of generality, Equation (10) can be written as

$$\mu = K_{TD}K_{DD}\left(\Phi\left(\frac{\phi_{f2}+\phi}{\sigma}\right) - \Phi\left(\frac{\phi_{f2}-\phi}{\sigma}\right)\right). \tag{11}$$

For the pattern-based PD proposed in [12], K_{DD} is 2 in case 1 because there are two judgment outputs in the single transition. K_{DD} also doubles in other cases, and the average K_{DD} is 1. So, the total output μ of the pattern-based PD is double that of a conventional MMPD, which can also be derived by using the same method as Equation (10). In pursuit of higher gain, we adopt a pattern-based PD in our system, and the MMPD mentioned later refers to pattern-based PD unless otherwise specified.

So, the gain expression of the MMPD is

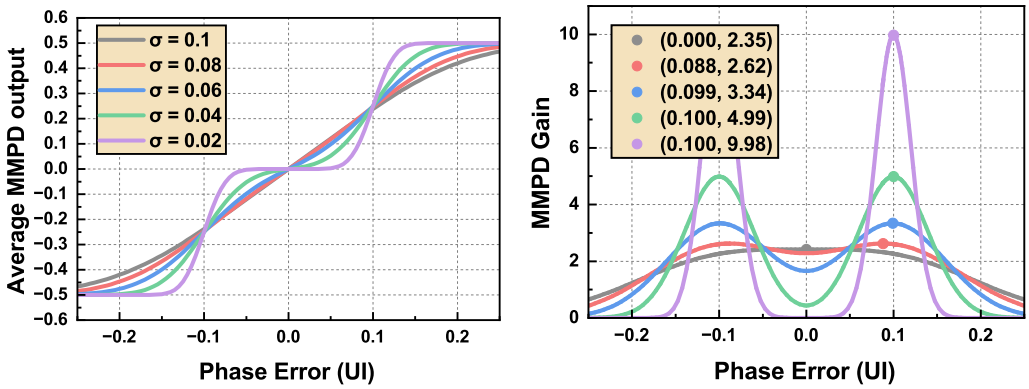
$$K_{MMPD} = \frac{\partial\mu}{\partial\phi} = \frac{K_{TD}K_{DD}}{\sqrt{2\pi}\sigma}\left(e^{-\frac{1}{2}\left(\frac{\phi_{f2}+\phi}{\sigma}\right)^2} + e^{-\frac{1}{2}\left(\frac{\phi_{f2}-\phi}{\sigma}\right)^2}\right). \tag{12}$$

It can be proved that for a certain case, the maximum gain of the MMPD occurs at $\phi_{f2} = 0$ and $\phi = 0$, which is

$$K_{MMPDmax} = \frac{2K_{TD}K_{DD}}{\sqrt{2\pi}\sigma} = \frac{1}{\sqrt{2\pi}\sigma}. \tag{13}$$

Equation (13) reveals that the maximum gain of the MMPD is determined by jitter only. For $\phi_{f2} \neq 0$, the peak gain occurs at $\phi = 0$ if $\sigma \geq \phi_{f2}$, and it moves to ϕ_{f2} gradually as σ

decreases. Figure 6 depicts the MMPD output and gain versus sampling phase error under different σ for $\phi_{f2} = 0.1UI$. Figure 6b gives the peak value for each curve.



(**a**) (**b**)

Figure 6. (**a**) The MMPD output characteristic under different σ, (**b**) the MMPD gain under different σ.

In order to quantify the relationship between reference voltage and PD output, a segmented linear function is employed to fit the waveform, from which the fuzzy phase is derived as

$$\phi_{f2} = \frac{V_{avg} - V_{ref}}{k}, \tag{14}$$

where V_{avg} is the amplitude of average crossing voltage at the intersection of 011 and 110 patterns, and the intersection instant is the ideal sampling phase

$$k = \begin{cases} \dfrac{V_{avg}}{0.5UI} & , V_{ref} \le V_{avg} \\ \dfrac{V_h - V_{avg}}{0.5UI} & , V_{avg} < V_{ref} \le V_h \end{cases} \tag{15}$$

and V_h is the average voltage of level "1" as shown in Figure 7.

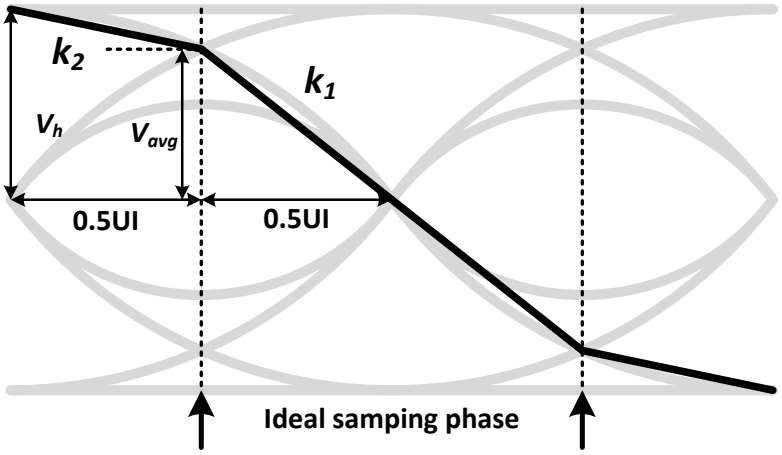


Figure 7. Segmented linear function to fit the waveform.

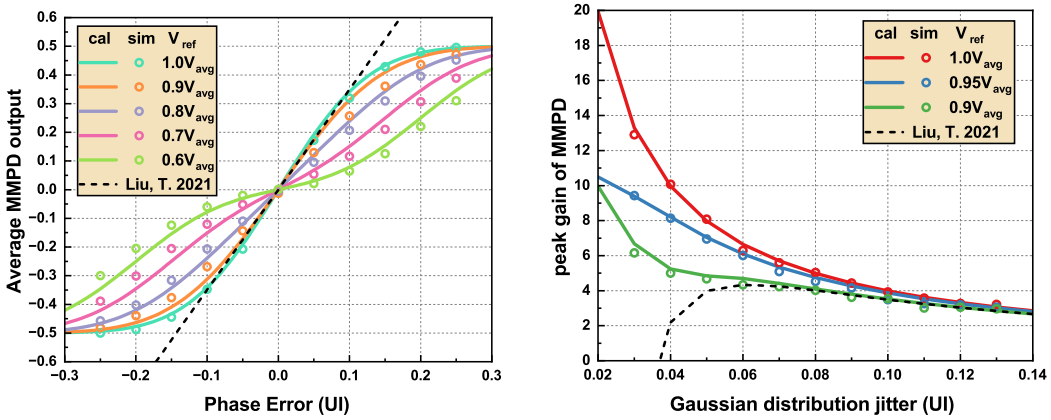
Substituting (14) into (11) and (12), we have

$$\mu = K_{TD}K_{DD}\left(\Phi\left(\frac{V_{avg} - V_{ref} + k\phi}{k\sigma}\right) - \Phi\left(\frac{V_{avg} - V_{ref} - k\phi}{k\sigma}\right)\right) \tag{16}$$

$$K_{MMPD} = \frac{K_{TD}K_{DD}}{\sqrt{2\pi}\sigma}\left(e^{-\frac{1}{2}\left(\frac{V_{avg}-V_{ref}+k\phi}{k\sigma}\right)^2} + e^{-\frac{1}{2}\left(\frac{V_{avg}-V_{ref}-k\phi}{k\sigma}\right)^2}\right). \tag{17}$$

To verify the expression, we establish a complete wireline transceiver system in Simulink. In this system, Gaussian-distributed jitter, with a standard deviation σ of 0.1 UI, is introduced into the input signal received by the receiver. By sweeping the sampling time of the CDR recovery clock and monitoring the PD output signal, the output characteristic curve is obtained, and the gain is the derivative of the output value with respect to the sampling phase.

Figure 8 presents the comparison between calculated and simulated results with little DJ. For comparisons with previous work, the results in [18] are also plotted. Figure 8a depicts the MMPD output characteristic at different V_{ref} whose $V_{avg} = V_h$. The calculated results are higher than the simulated because the fitting ϕ_{f2} is always lower than the actual value. As the analysis in [18], when $|\phi| < 0.1$ UI, their calculation results are close to the simulation results, and our calculation results at $V_{ref} = 0.9V_{avg}$, because ϕ_{f2} is equal to the drift bit width. However, when the phase error exceeds this range, our model matches the simulation results better. Moreover, they do not give the calculation model under different reference voltages. When the reference voltage setting is changed, the trend of the calculation results of our model matches the simulation results. Figure 8b shows the relationship between the MMPD peak gain and the Gaussian-distributed jitter σ at different V_{ref}, from which it can be seen that the gain is inversely proportional to the Gaussian-distributed jitter σ when $V_{ref} = V_{avg}$, and when the σ is large, peak gain under different V_{ref} values will approach $\frac{1}{\sqrt{2\pi}\sigma}$, because the exponent in Equation (12) becomes closer to 0. In addition, Figure 8b shows that the gain calculated in [18] matches the simulation results when the jitter is large, and the error is larger for smaller jitter. This is because it only considers the gain at the phase error of 0, while for smaller jitter, the MMPD peak gain dose not occur at this point, as shown in Figure 6, and our model shows better matching in a wider range.



(**a**) (**b**)

Figure 8. (**a**) MMPD output characteristic at different V_{ref} and the calculation result in [18], (**b**) the MMPD peak gain under different σ and the calculation result in [18].

Furthermore, to take DJ into account, the deterministic phase offset ϕ_D is added to ϕ in Equation (11), which can be written as

$$\mu = K_{TD}K_{DD}\left(\Phi\left(\frac{\phi_{f2}+\phi+\phi_D}{\sigma}\right) - \Phi\left(\frac{\phi_{f2}-\phi-\phi_D}{\sigma}\right)\right). \tag{18}$$

Taking inter-symbol interference (ISI) as an example, the previous bits residual state affects the current sampling voltage, which may cause different error signals in the MMPD. Define the residual voltage as V_{res}; then, $\phi_D = V_{res}/k$.

The input signal with ISI is simulated as the eye diagram shown in Figure 9 whose $V_h = 1.4V_{avg}$ and the range of crossing voltage at the intersection of the 011 and 110 patterns is from 0.88 to $1.12V_{avg}$. For simplicity, we simplify the probability distribution of the V_{res}

into 25% of $-0.09V_{avg}$, 50% of 0 and 25% of $+0.09V_{avg}$. So, our modified fitting function in this case can be written as

$$\mu = K_{TD}K_{DD}\left(\Phi\left(\frac{V_{avg} - V_{ref} + V_{res} + k\phi}{k\sigma}\right) - \Phi\left(\frac{V_{avg} - V_{ref} - V_{res} - k\phi}{k\sigma}\right)\right)Pr(V_{res}). \quad (19)$$

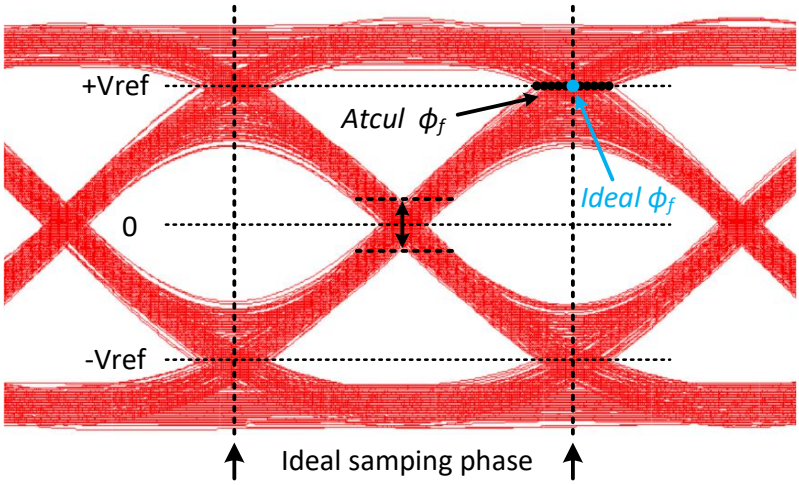
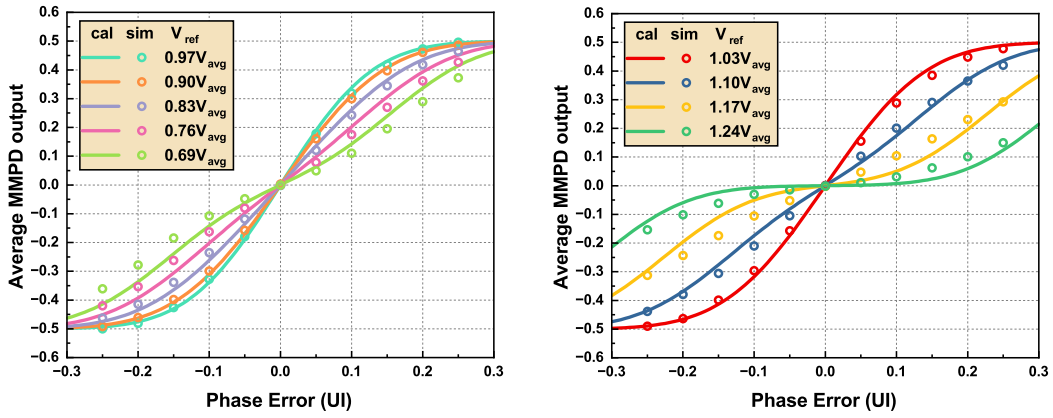


Figure 9. Simulated eye diagram with rough equalization.

Figure 10 shows the calculated MMPD output results without or with modification versus the simulated, from which we can find that calculations with modification fit the simulation better than without modification when $V_{ref} > V_{avg}$, because the low slope makes the PD more sensitive to V_{ref}, and the introduction of ISI reduces the sensitivity and smooths the output curve. The difference is not significant when $V_{ref} < V_{avg}$, which may be due to the high linearity of function within this range, and the effects of ISI with a mean of 0 cancel out.

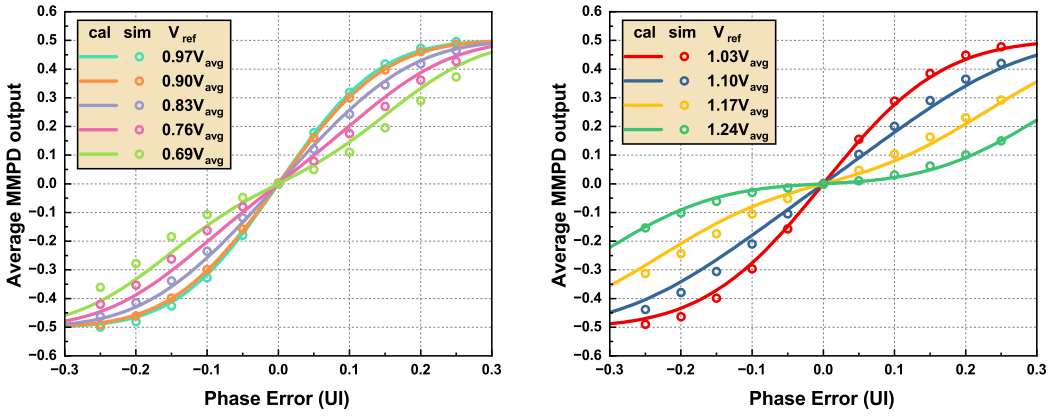
Figure 11 depicts the peak gain of the MMPD with ISI versus the Gaussian distribution jitter σ under different V_{ref} before and after function modification, from which it can be seen that the peak gain has significantly decreased at low σ, when V_{ref} is close to V_{avg}, because the ISI introduces an equivalent ϕ_{f2} which will never be zero.

It should be noted that for more severe ISI, estimating the distribution of V_{res} will become complicated, and the deviation between the model calculation results and the circuit simulation results may become too large if the estimation is inaccurate.



(**a**) (**b**)

Figure 10. *Cont.*



(**c**) (**d**)

Figure 10. MMPD output characteristic: (**a**) $V_{ref} < V_h$ without modification, (**b**) $V_{ref} > V_h$ without modification, (**c**) $V_{ref} < V_h$ with modification, (**d**) $V_{ref} > V_h$ with modification.

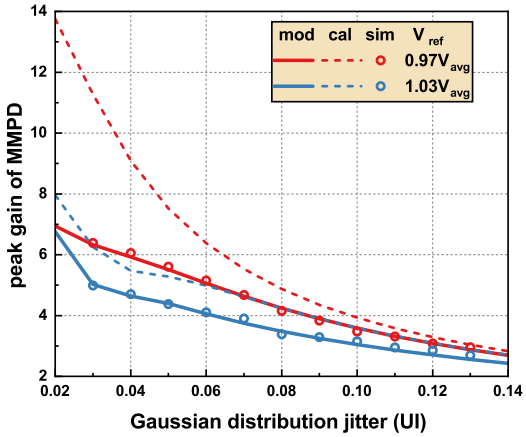


Figure 11. Peak gain of MMPD with ISI under different σ.

3. Small Signal Model of MM-CDR

3.1. The Architecture of MMPD-Based Digital CDR

When the ADC-based receiver is preferred in a high-speed wireline transceiver, the digital CDR is a more attractive solution compared with the analog implementation.

The digital CDR loop which includes the MMPD, decimation block, frequency integrator, phase integrator and phase interpolator is shown in Figure 12. In this work, the data rate of the transceiver implemented in 28 nm CMOS is 32 Gb/s. The MMPD receives 64 lanes 500 Mb/s parallel sign data and sign error information. The decimation block is used to reduce the baud rate phase error samples to a rate compatible with high-resolution digital signal processing. The proportional path through K_P combined with the integral path through K_I is used to filter the phase detector decisions. The phase interpolator uses a multi-bit digital control bus to adjust the phase of the ADC sampling clocks.

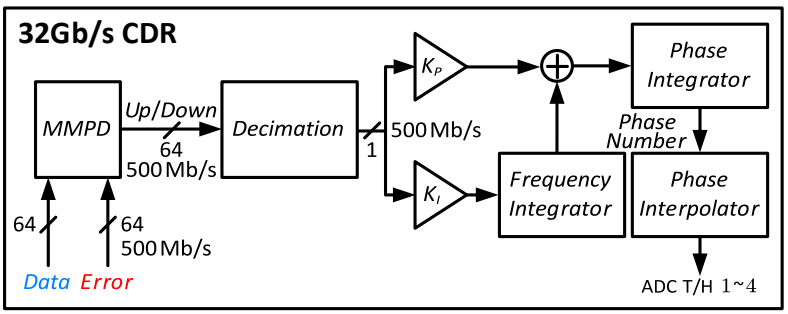


Figure 12. The architecture of 32 Gb/s MMPD-based digital CDR.

3.2. Linearized Analysis of CDR System

In order to analyze the design of the digital CDR, the digital CDR needs to be linearly modeled and the linearized model, equivalent to the structure in Figure 12, is shown in Figure 13, where K_{PD} is the gain of the MMPD, K_D is the decimation gain, K_P is the gain of the proportional path, K_I is the gain of the integral path, K_{PI} is the gain of the phase interpolator, and z^{-N} is the delay of the digital CDR loop. These parameters are listed in Table 2 and described in the following content.

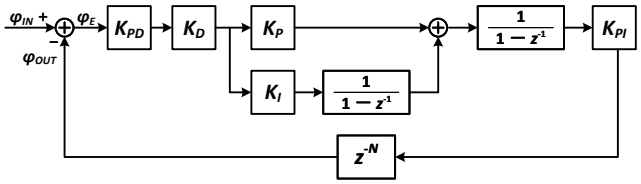


Figure 13. The linearized model of 32 Gb/s MMPD-based digital CDR.

Table 2. Digital MM-CDR parameters.

Parameter	Value
K_{PD}	13.3, 9.4, 6.8 per UI under σ = 0.03 UI 10, 8.2, 5.2 per UI under σ = 0.04 UI
K_D	$0.54 \times 64 = 34.56$
K_P	2^{-7}
K_I	2^{-12}
K_{PI}	1 UI / 2^5 bit
N	5

The values of K_{PD} are obtained from the results shown in Figure 8b. We assume that σ is equal to 0.03 UI and 0.04 UI to demonstrate the loop performance under different Gaussian jitter. In order to verify the effect of reference voltage on the circuit performance, different values are set to obtain their respective gains of the MMPD, as listed in Table 2.

We adopt voting to achieve decimation, since it is beneficial to reduce the latency of the loop, and the decimation factor is 64. The voting gain K_D can be obtained by co-simulation with the MMPD, and the value of voting gain K_D is around 0.54 when $V_{ref} = V_{avg}$ through simulation.

The values of K_P and K_I are programmable to meet various requirements of CDR loop characteristics in different applications, such as the bandwidth of the CDR loop and the range of frequency deviation tracking .

The parameter K_{PI} corresponds to the resolution of the phase interpolator in units of UI per bit, which is chosen as 5-bit in our system by considering the performance and complexity of the circuit.

The performances of the CDR loop that we care about are mainly the jitter transfer function and jitter tolerance (JTOL). The loop gain of this linearized model can be analyzed as follows:

$$L\left(z^{-1}\right) = \frac{\phi_{OUT}}{\phi_E} = \frac{K_{PD}K_DK_{PI}}{1-z^{-1}}\left(K_P + \frac{K_I}{1-z^{-1}}\right)z^{-N}. \tag{20}$$

The expression of the jitter transfer function is

$$H\left(e^{-j\omega}\right) = \frac{\phi_{OUT}}{\phi_{IN}} = \frac{L\left(e^{-j\omega}\right)}{1+L\left(e^{-j\omega}\right)}. \tag{21}$$

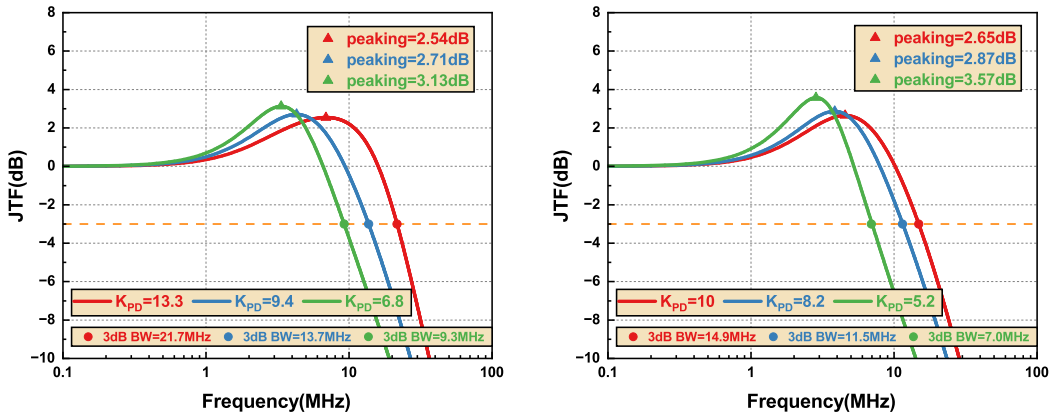
The CDR in this design needs to meet the JESD204C protocol with a BER requirement of 1×10^{-15}, so the expression of JTOL is

$$JT\left(e^{-j\omega}\right) = \frac{\phi_{IN}}{\phi_E}\left(1 - \frac{15.88\sigma}{T_{UI}}\right) = \left(1 + L\left(e^{-j\omega}\right)\right)\left(1 - \frac{15.88\sigma}{T_{UI}}\right). \tag{22}$$

4. Simulation Results

According to the linearization analysis of the MMPD and digital MM-CDR in Sections 2 and 3, we perform jitter transfer function and jitter tolerance simulations on the digital MM-CDR loop.

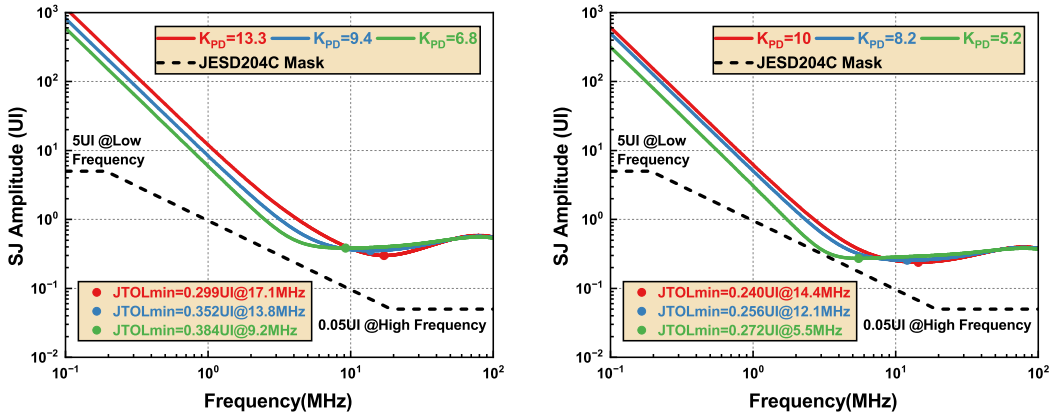
Figure 14a,b plot the jitter transfer function performance under Gaussian jitter standard deviations of the 0.03 UI and 0.04 UI. It can be seen that the greater the gain of the MMPD, the wider the bandwidth of jitter transfer function and the smaller the jitter peaking. It can be observed that when σ equals 0.04 UI, the peaking takes on values of 2.65, 2.87, and 3.57 dB and the corresponding bandwidths are 14.9, 11.5, and 7.0 MHz. When σ is equal to 0.03 UI, the gain of the MMPD is higher, resulting in better peaking and bandwidth performance. The peaking takes on values of 2.54, 2.71, and 3.13 dB, and the corresponding bandwidths are 21.7, 13.7, and 9.3 MHz.



(**a**) (**b**)

Figure 14. Jitter transfer function of digital MM-CDR under Gaussian jitter standard deviation of (**a**) 0.03 UI and (**b**) 0.04 UI.

It can be seen from Figure 15a,b that all the settings meet the JESD204C jitter tolerance limit. Whether σ is equal to 0.03 UI or 0.04 UI, the higher the gain of the MMPD, the greater the margin of the JTOL. Although JTOLmin will be smaller, K_P and K_I can be adjusted to improve it. When σ is equal to 0.04 UI, the minimum JTOL is 0.240 UI at 14.4 MHz, which is far more than the 0.05 UI required by JESD204C protocol. JTOL remains around 0.32 UI for the high-frequency condition above 100 MHz. When σ is equal to 0.03 UI, the lowest JTOL is 0.299 UI at 17.1 MHz and JTOL remain around 0.48 UI for the high-frequency condition above 100 MHz.



(**a**) (**b**)

Figure 15. Jitter tolerance of digital MM-CDR under Gaussian jitter standard deviation of (**a**) 0.03 UI and (**b**) 0.04 UI.

5. Conclusions

In this paper, we present a detailed analysis of the MM-CDR system, focusing on the development of a linearized model for the MMPD. The analysis reveals that the reference voltage in the MMPD plays a critical role in determining its gain and overall performance. When the reference voltage is set equal to the amplitude of average crossing voltage at the intersection of 011 and 110 patterns, the maximum MMPD gain and optimal JTOL can be achieved, which is determined by the jitter in the system. We further extend the linearized MMPD model into a complete MM-CDR system and evaluate its performance in simulations. The results confirm that this system complies with the JESD204C standard [19] when reference voltage is appropriate and can achieve better JTOL with a higher MMPD gain.

In summary, the proposed linearized model provides an effective approach for evaluating and optimizing the MM-CDR system during the design stage. This method allows for a more accurate prediction of system performance under various jitter conditions, providing valuable insights for the design of ADC-based wireline receivers in high-speed data transmission systems.

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References

1. Mueller, K.; Muller, M. Timing Recovery in Digital Synchronous Data Receivers. *IEEE Trans. Commun.* **1976**, *24*, 516–531. [CrossRef]
2. Spagna, F.; Chen, L.; Deshpande, M.; Fan, Y.; Gambetta, D.; Gowder, S.; Iyer, S.; Kumar, R.; Kwok, P.; Krishnamurthy, R.; et al. A 78 mW 11.8 Gb/s serial link transceiver with adaptive RX equalization and baud-rate CDR in 32 nm CMOS. In Proceedings of the 2010 IEEE International Solid-State Circuits Conference—(ISSCC), San Francisco, CA, USA, 7–11 February 2010; pp. 366–367. [CrossRef]
3. Shi, L.; Gai, W.; Tang, L.; Xiang, X.; He, A. Hardware-efficient slope-error algorithm based PAM4 baud rate CDR scheme for 40 Gb/s receiver. *Electron. Lett.* **2018**, *54*, 1020–1022. [CrossRef]
4. Sonntag, J.; Stonick, J. A Digital Clock and Data Recovery Architecture for Multi-Gigabit/s Binary Links. *IEEE J. Solid-State Circuits* **2006**, *41*, 1867–1875. [CrossRef]
5. Park, M.J.; Kim, J. Pseudo-Linear Analysis of Bang-Bang Controlled Timing Circuits. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2013**, *60*, 1381–1394. [CrossRef]
6. Liang, J.; Sheikholeslami, A.; Tamura, H.; Ogata, Y.; Yamaguchi, H. Loop Gain Adaptation for Optimum Jitter Tolerance in Digital CDRs. *IEEE J. Solid-State Circuits* **2018**, *53*, 2696–2708. [CrossRef]
7. Ge, X.; Chen, Y.; Zhao, X.; Mak, P.I.; Martins, R.P. Analysis and Verification of Jitter in Bang-Bang Clock and Data Recovery Circuit With a Second-Order Loop Filter. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2019**, *27*, 2223–2236. [CrossRef]
8. Shu, Z.; Huang, S.; Li, Z.; Yin, P.; Zang, J.; Fu, D.; Tang, F.; Bermak, A. A 5–13.5 Gb/s Multistandard Receiver With High Jitter Tolerance Digital CDR in 40-nm CMOS Process. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2020**, *67*, 3378–3388. [CrossRef]
9. Ting, C.; Liang, J.; Sheikholeslami, A.; Kibune, M.; Tamura, H. A Blind Baud-Rate ADC-Based CDR. *IEEE J. Solid-State Circuits* **2013**, *48*, 3285–3295. [CrossRef]
10. Han, J.; Sutardja, N.; Lu, Y.; Alon, E. Design Techniques for a 60-Gb/s 288-mW NRZ Transceiver With Adaptive Equalization and Baud-Rate Clock and Data Recovery in 65-nm CMOS Technology. *IEEE J. Solid-State Circuits* **2017**, *52*, 3474–3485. [CrossRef]
11. Lee, Y.S.; Ho, W.H.; Chen, W.Z. A 25-Gb/s, 2.1-pJ/bit, Fully Integrated Optical Receiver With a Baud-Rate Clock and Data Recovery. *IEEE J. Solid-State Circuits* **2019**, *54*, 2243–2254. [CrossRef]

12. Park, S.; Choi, Y.; Sim, J.; Choi, J.; Park, H.; Kwon, Y.; Kim, C. A 0.83 pJ/b 52 Gb/s PAM-4 Baud-Rate CDR with Pattern-Based Phase Detector for Short-Reach Applications. In Proceedings of the 2023 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 19–23 February 2023; pp. 118–120. [CrossRef]
13. Francese, P.A.; Toifl, T.; Buchmann, P.; Brändli, M.; Menolfi, C.; Kossel, M.; Morf, T.; Kull, L.; Andersen, T.M. A 16 Gb/s 3.7 mW/Gb/s 8-Tap DFE Receiver and Baud-Rate CDR With 31 kppm Tracking Bandwidth. *IEEE J. Solid-State Circuits* **2014**, *49*, 2490–2502. [CrossRef]
14. Dokania, R.; Kern, A.; He, M.; Faust, A.; Tseng, R.; Weaver, S.; Yu, K.; Bil, C.; Liang, T.; O'Mahony, F. 10.5 A 5.9 pJ/b 10 Gb/s serial link with unequalized MM-CDR in 14 nm tri-gate CMOS. In Proceedings of the 2015 IEEE International Solid-State Circuits Conference—(ISSCC), San Francisco, CA, USA, 22–26 February 2015; pp. 1–3. [CrossRef]
15. Mehrotra, P.; Maity, S.; Sen, S. An Improved Update Rate CDR for Interference Robust Broadband Human Body Communication Receiver. *IEEE Trans. Biomed. Circuits Syst.* **2019**, *13*, 868–879. [CrossRef] [PubMed]
16. Choi, M.C.; Ko, H.G.; Oh, J.; Joo, H.Y.; Lee, K.; Jeong, D.K. A 0.1-pJ/b/dB 28-Gb/s Maximum-Eye Tracking, Weight-Adjusting MM CDR and Adaptive DFE with Single Shared Error Sampler. In Proceedings of the 2020 IEEE Symposium on VLSI Circuits, Honolulu, HI, USA, 16–19 June 2020; pp. 1–2. [CrossRef]
17. Yoo, B.J.; Lim, D.H.; Pang, H.; Lee, J.H.; Baek, S.Y.; Kim, N.; Choi, D.H.; Choi, Y.H.; Yang, H.; Yoon, T.; et al. 6.4 A 56 Gb/s 7.7 mW/Gb/s PAM-4 Wireline Transceiver in 10 nm FinFET Using MM-CDR-Based ADC Timing Skew Control and Low-Power DSP with Approximate Multiplier. In Proceedings of the 2020 IEEE International Solid-State Circuits Conference—(ISSCC), San Francisco, CA, USA, 16–20 February 2020; pp. 122–124. [CrossRef]
18. Liu, T.; Li, T.; Lv, F.; Liang, B.; Zheng, X.; Wang, H.; Wu, M.; Lu, D.; Zhao, F. Analysis and Modeling of Mueller–Muller Clock and Data Recovery Circuits. *Electronics* **2021**, *10*, 1888. [CrossRef]
19. *JESD204C*; Serial Interface for Data Converters. JEDEC Solid State Technology Association: Arlington, VA, USA, 2017.